



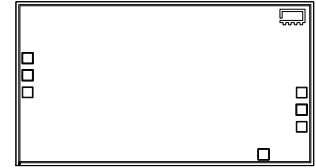
MMIC DIE

Wideband Amplifier **AVA-183MP-D+**

50Ω DC to 18 GHz

THE BIG DEAL

- Wideband, DC to 18 GHz
- P1dB, +23.2 dBm Typ. at 10 GHz
- OIP3, +29.5 dBm Typ. at 10 GHz
- Reverse Isolation, 27 dB Typ.



+RoHS Compliant

The +Suffix identifies RoHS Compliance.
See our website for methodologies and qualifications

APPLICATIONS

- 5G MIMO and Back Haul Radio Systems
- Satellite Communications
- Test and Measurement Equipment
- Radar, EW, and ECM Defense Systems

SEE ORDERING INFORMATION ON THE LAST PAGE

PRODUCT OVERVIEW

AVA-183MP-D+ is a GaAs PHEMT MMIC wideband distributed amplifier operating from 0.05 to 18 GHz. The amplifier provides 14.5 dB of Gain, +23 dBm P1dB, and +29.5 dBm OIP3 typical performance while operating from an +8V supply with 160mA current consumption. The amplifier has excellent input and output impedance matches which makes for easy cascading with other devices in multi-chip modules. The AVA-183MP-D+ performance characteristics are ideal for use in wideband Defense Systems and Test and Measurement Equipment.

KEY FEATURES

Feature	Advantages
Wideband: DC to 18 GHz <ul style="list-style-type: none"> • 20.4 dB Gain Typ. at 50 MHz • 14.2 dB Gain Typ. at 18 GHz 	Suitable for wide bandwidth Defense and Test and Measurement application as well as narrow band performance driven applications.
Medium Power <ul style="list-style-type: none"> • P1dB +23.5 dBm ± 1.5 dB from 0.05 to 18 GHz 	Suitable as a driver amplifier in receiver/transmitter chains.
Reverse Isolation, 27 dB Typ.	Isolates adjacent circuitry without need for an external expensive isolator.
Good Input and Output Return Loss <ul style="list-style-type: none"> • 16 dB typical 	Eliminates need for external matching circuit providing published Return Loss.
Unpackaged die	Suitable for chip and wire hybrid assemblies.

REV. OR
ECO-014454
AVA-183M-D+
GY/RS/CP
220804





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ELECTRICAL SPECIFICATIONS¹ AT 25°C, VDD = +8V, IDD = 160mA & Zo = 50Ω UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	VDD = +8V			Units
		Min.	Typ.	Max.	
Frequency Range		0.05		18	GHz
Gain	0.05		20.4		dB
	5		15.9		
	10		14.5		
	15		14.6		
	18		14.2		
Input Return Loss	0.05		10		dB
	5		22		
	10		14		
	15		11		
	18		10		
Output Return Loss	0.05		9		dB
	5		17		
	10		19		
	15		18		
	18		21		
Reverse Isolation	0.05 - 18		27		dB
Output Power at 1 dB Compression ²	0.05		25.4		dBm
	5		24.4		
	10		23.2		
	15		22.9		
	18		22.9		
Output Third-Order Intercept (Pout = +5 dBm/Tone)	0.05		38.6		dBm
	5		33.4		
	10		29.5		
	15		26.8		
	18		25.2		
Noise Figure	0.05		5.4		dB
	5		2.0		
	10		2.8		
	15		3.5		
	18		4.4		
Device Operating Voltage (VDD)			+8		V
Device Operating Current (IDD)		–	160	–	mA
Device Gate Voltage (VGG)		–	-1.3	–	V
Device Gate Current (IGG)		–	-0.5	–	mA
Thermal Resistance, Junction-to-Ground Lead (ΘJC)		–	17.3	–	°C/W

1. Die is soldered and measured in a die characterization test board. See characterization circuit (Fig. 1). Starting frequency of this device is dependent on the input blocking capacitor value.
2. DC current increases to 258mA Typ. at P1dB.



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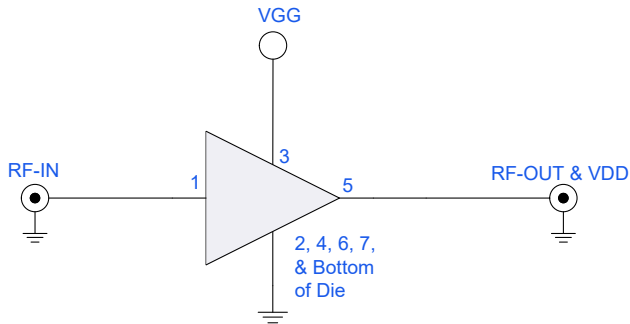
MAXIMUM RATINGS³

Parameter	Ratings
Operating Temperature (ground lead)	-40°C to +85°C
Junction Temperature	+150°C ⁴
Total Power Dissipation	2.8W
Input Power (CW)	+21dBm
DC Voltage on RF-OUT & VDD	+14V
DC Voltage on VGG	-2V to -0.5V
Current IDD	350mA
Current IGG	-1.5mA to 0mA

3. Permanent damage may occur if these limits are exceeded.

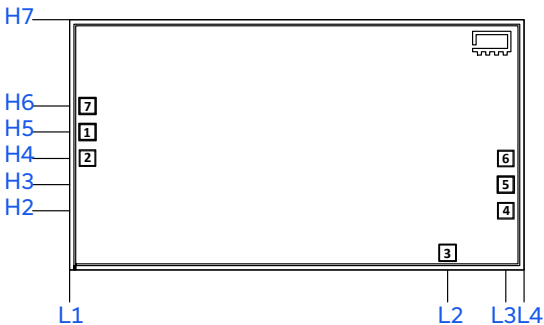
4. $T_j = +85^\circ\text{C} + (VDD) \cdot (IDD) \cdot (\theta_{JC}) = +107^\circ\text{C}$. Keeping T_j below $+107^\circ\text{C}$ will ensure $MTTF > 100$ Years

SIMPLIFIED SCHEMATIC AND PAD DESCRIPTION



Function	Pad #	Description
RF-IN	1	RF Input Pad
VGG	3	Gate Bias Pad
RF-OUT & VDD	5	RF Output and Drain Pad
GROUND	2, 4, 6, 7 & Bottom of Die	The bond pads are connected to backside through vias and do not require wire-bond connections to ground.

BONDING PAD POSITION



DIMENSION IN μm, TYP.

L1	L2	L3	L4
103	2174	2508	2614

H1	H2	H3	H4	H5	H6	H7
98	340	490	640	793	943	1438

Thickness	Die size	Pad size 1,2,4,5,6 & 7	Pad size 3
100	2614 x 1438	85 x 85	93 x 93



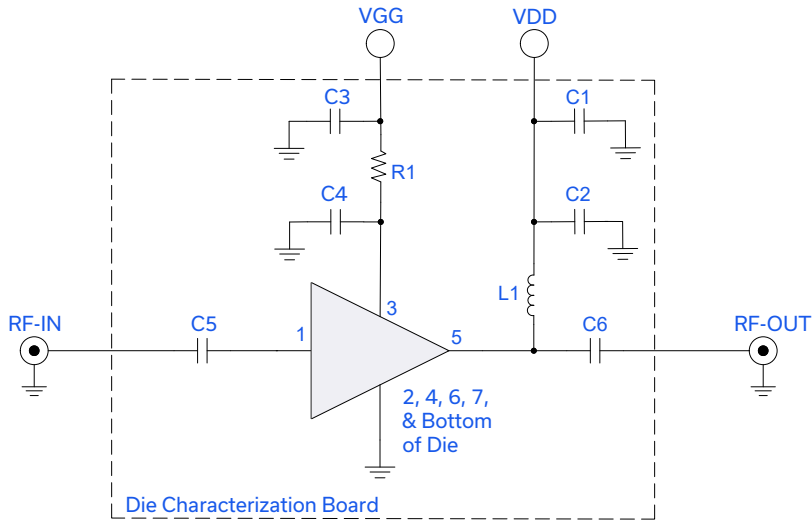


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CHARACTERIZATION & APPLICATION TEST CIRCUIT



Component	Value	Size	Part Number	Manufacturer
C2, C3, C5 & C6	0.1uF	0402	0402BB104KG500	Passive Plus
C4	100pF	15 x 15mil	LSA1515B101M2H5C-F	Presidio
C1	NA	NA	Not Used	NA
L1	0.17uH	60 x 40mil	CC20T44K240G5-C	Piconics
R1	1kOhm	0402	RR0510P-102-D	Susumu

Fig 1. Characterization & Application Circuit

Note: This block diagram is used for characterization. (Die is attached and wire-bonded on die characterization test board). Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3) and Noise Figure are measured using Agilent's N5242A PNA-X Microwave Network Analyzer.

Conditions:

1. VDD = +8V
2. VG is set to obtain desired IDD as shown in specification table.
3. Gain and Return Loss: Pin= -25 dBm
4. Output IP3 (OIP3): Two Tones, spaced 1 MHz apart, +5 dBm/Tone at output.

Power ON Sequence:

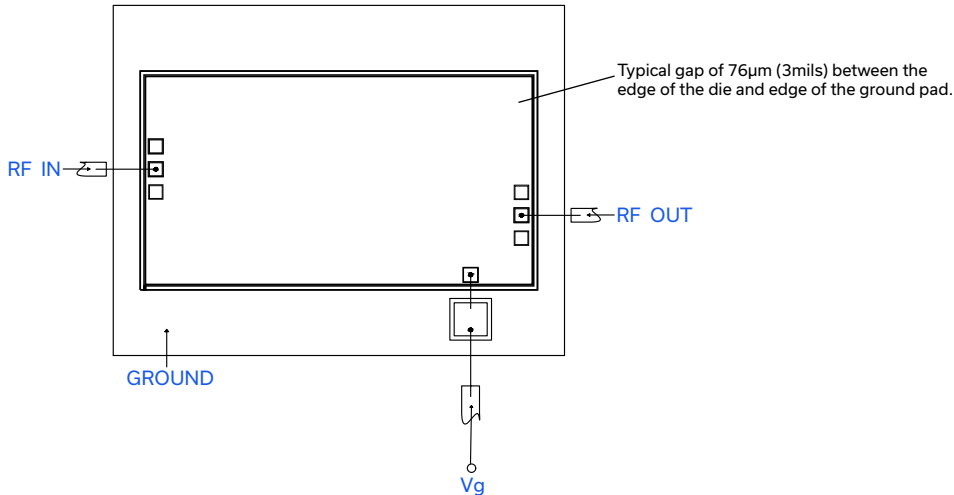
- 1) Set VGG = -1.8V. Apply VGG.
- 2) Set VDD = +8V. Apply VDD.
- 3) Adjust VGG until IDD = 160mA (Typically, VGG = -1.3V)
- 4) Apply RF Signal.

Power OFF Sequence:

- 1) Turn off RF Signal.
- 2) Adjust VGG down to -1.8V
- 3) Turn off VDD.
- 4) Turn off VGG.




ASSEMBLY DIAGRAM



Note: Tested on die characterization board with following bond lengths:

1. Typical bond length for RF-IN: 305µm (12mils)
2. Typical bond length for RF-OUT & VDD: 330µm (13mils)
3. Typical bond lengths from die, capacitor, and VGG were kept as short as possible
4. 30 pF capacitor can be added as shown for increased stability.

ASSEMBLY AND HANDLING PROCEDURE

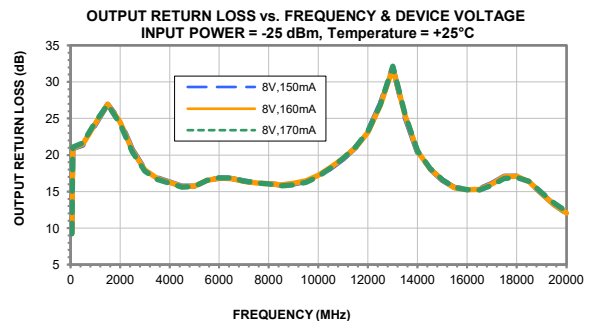
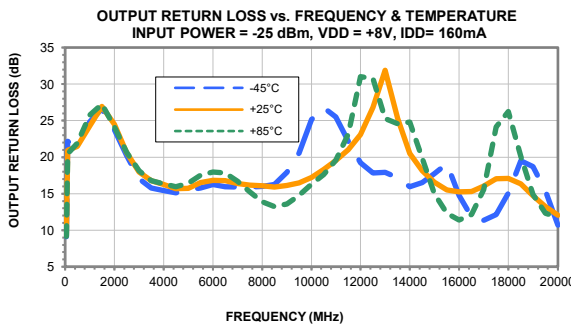
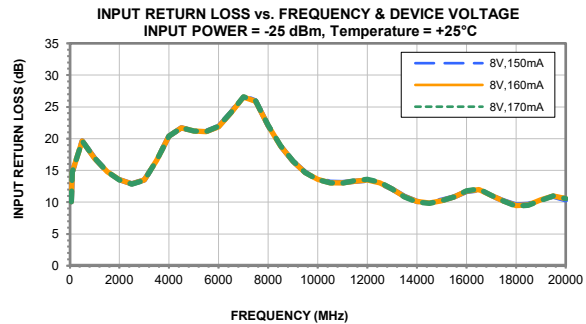
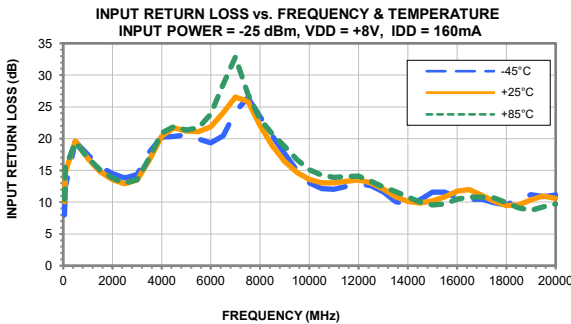
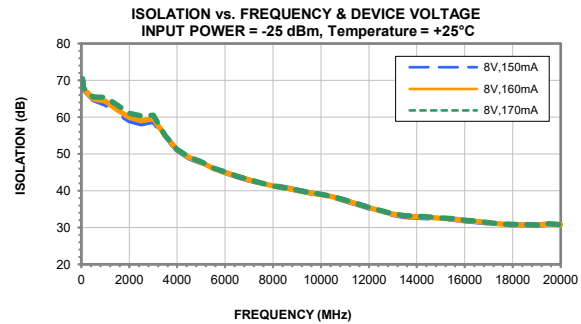
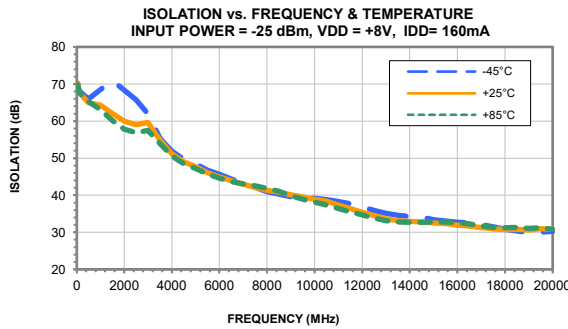
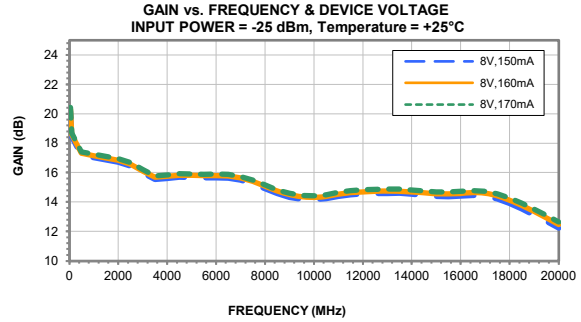
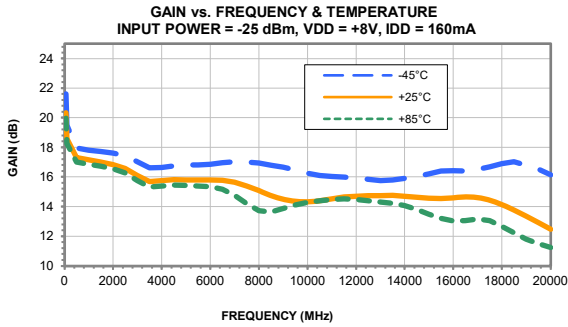
1. **Storage**
Die should be stored in a dry nitrogen purged desiccators or equivalent.
2.  **ESD**
MMIC PHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.
3. **Die Handling and Attachment**
Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.
4. **Wire Bonding**
Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the Die gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wire length and bond wire height should be kept as short as possible unless specified by the Assembly Drawing to minimize performance degradation due to undesirable series inductance.



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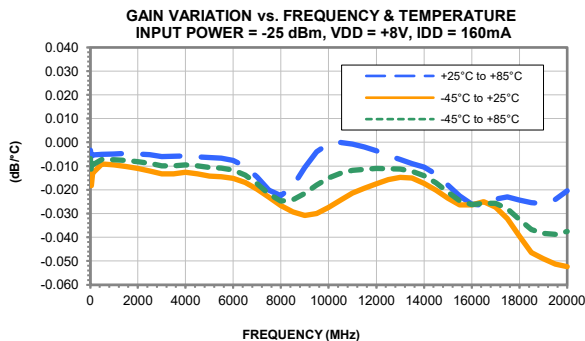
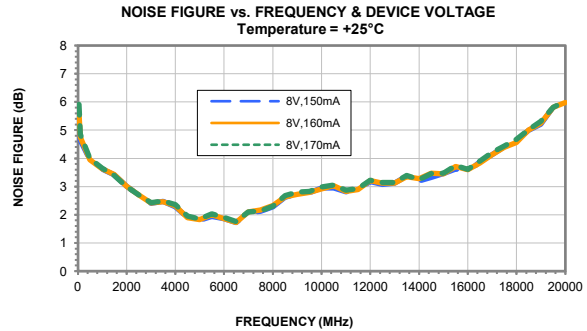
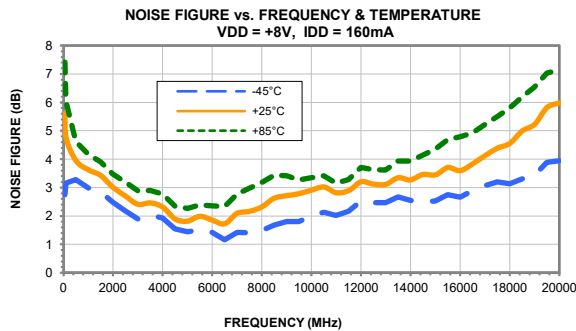
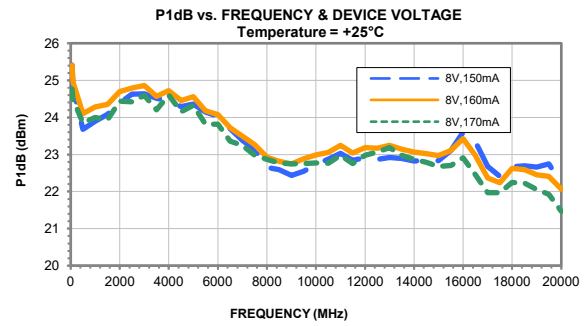
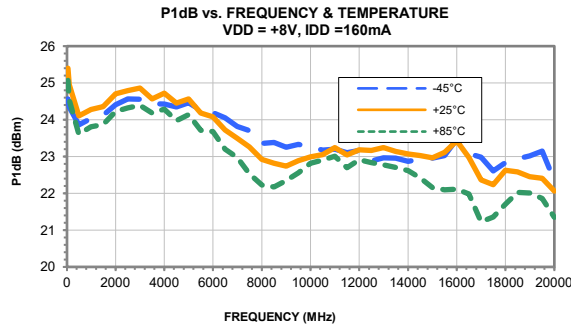
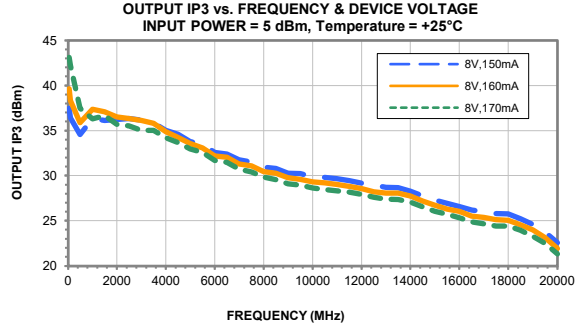
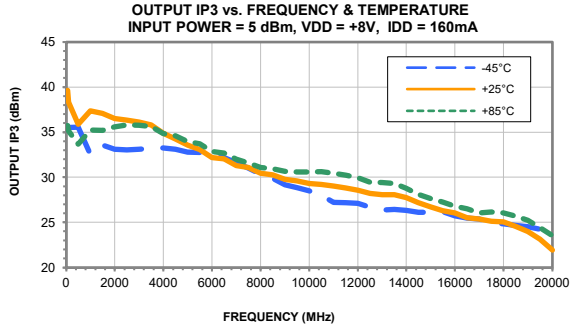




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ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASH BOARD.

Performance Data	Data Table Swept Graphs S-Parameter (S2P Files) Data Set with and without port extension(.zip file)								
Case Style	Die								
Die Ordering and packaging information	<table border="0"> <tr> <td>Quantity, Package</td> <td>Model No.</td> </tr> <tr> <td>Gel - Pak: 5,10,50,100 KGD*</td> <td>AVA-183MP-DG+</td> </tr> <tr> <td>Medium[†], Partial wafer: KGD*<570</td> <td>AVA-183MP-DP+</td> </tr> <tr> <td>Full wafer</td> <td>AVA-183MP-DF+</td> </tr> </table> <p>[†]Available upon request contact sales representative Refer to AN-60-067</p>	Quantity, Package	Model No.	Gel - Pak: 5,10,50,100 KGD*	AVA-183MP-DG+	Medium [†] , Partial wafer: KGD*<570	AVA-183MP-DP+	Full wafer	AVA-183MP-DF+
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Gel - Pak: 5,10,50,100 KGD*	AVA-183MP-DG+								
Medium [†] , Partial wafer: KGD*<570	AVA-183MP-DP+								
Full wafer	AVA-183MP-DF+								
Die Marking	EL-AMP-7-2								
Die TB Reference	XM-C9A1-0404D								
Environmental Ratings	ENV80								

*Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a higher degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

NOTES

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
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