SN65LBC176-Q1 Differential Bus Transceiver

1 Features

- Qualified for automotive applications
- Bidirectional transceiver
- Meet or exceed the requirements of ANSI standard RS-485 and ISO 8482:1987(E)
- High-speed low-power LinBiCMOS circuitry
- Designed for high-speed operation in both serial and parallel applications
- Low skew
- Designed for multipoint transmission on long bus lines in noisy environments
- Very low disabled supply-current requirements: 200 µA maximum
- Wide positive and negative input/output bus voltage ranges
- Driver Output Capacity: ±60 mA
- Thermal-Shutdown Protection
- Driver positive-and negative-current limiting
- Open-Circuit Fail-Safe Receiver Design
- Receiver input sensitivity: ±200 mV max
- Receiver input hysteresis: 50 mV typical
- Operate from a single 5-V supply
- Glitch-free power-up and power-down protection

2 Description

The SN65LBC176 differential bus transceiver is a monolithic, integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard RS-485 and ISO 8482:1987(E).

The SN65LBC176 combines a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or VCC = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver. Both the driver and receiver are available as cells in the Texas Instruments LinASIC Library.

This transceiver is suitable for ANSI Standard RS-485 and ISO 8482:1987 (E) applications to the extent that they are specified in the operating conditions and characteristics section of this data sheet. Certain limits contained in the ANSI Standard RS-485 and ISO 8482:1987 (E) are not met or cannot be tested over the entire extended temperature range.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65LBC176-Q1	D (SOIC) (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

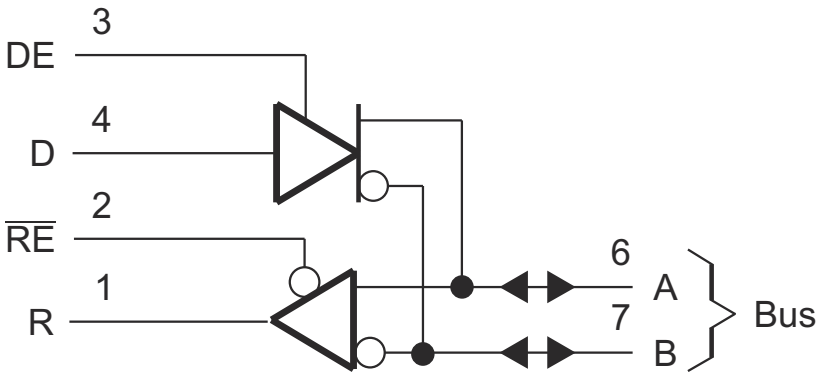


Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2003) to Revision B (January 2023)	Page
• Added the *Package Information* table, *Pin Configuration and Implementation*, *Thermal Information* table, *Device Functional Modes*, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted the *Ordering Information* table	1

4 Pin Configuration and Functions

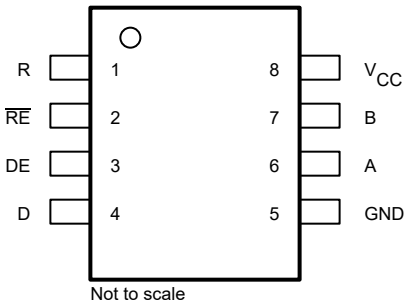


Figure 4-1. D Package, SOIC 8 Pins (Top View)

Table 4-1. Pin Functions

NO	NAME	TYPE	DESCRIPTION
1	R	O	Receive data output
2	$\overline{RE}$	I	Receiver enable, active low
3	DE	I	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Device ground
6	A	I/O	Bus I/O port, A (complementary to B)
7	B	I/O	Bus I/O port, B(complementary to A)
8	V_{CC}	P	5 V Supply Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		7	V
	Voltage range at any bus terminal	-10	15	V
	Input voltage, VI (D, DE, R, or $\overline{RE}$)	−0.3	V_{CC} + 0.5	V
T_A	Operating free-air temperature range	-40	125	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode),				12	V
					-7	V
V_{IH}	High-level input voltage,	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage,	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			60	mA
		Receiver			-400	µA
I_{OL}	Low-level output current	Driver			-60	mA
		Receiver			8	mA
T_A	Operating free-air temperature,		-40		125	°C

(1) Differential input /output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

5.3 Thermal Resistance Characteristics

THERMAL METRIC(1)		SN65LBC176-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics - Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = − 18 mA				-1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V	See Fig 2, (2)	1.1			V
$\|V_{OD2}\|$	Differential output voltage	R_L = 54 Ω	See Fig 1, (2)	1.1			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(1)	R_L = 54 Ω or 100 Ω See Fig 1				±0.2	V
V_{OC}	Common-mode output voltage					-1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(1)					±0.2	V
I_O	Output current	Output disabled, (3)	V_O = 12 V			1	mA
			V_O = -7 V			-0.8	mA
I_{IH}	High-level input current	V_I = 2.4 V				-100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				-100	µA
I_{OS}	Short-circuit output current	V_O = -7 V				-250	mA
		V_O = 0 V				-150	mA
		V_O = V_{CC}				250	mA
		V_O = 12 V				250	mA
I_{CC}	Supply current	V_I = 0 or V_{CC}, No Load	Receiver disabled and driver enabled			1.75	mA
			Receiver and driver disabled			0.25	mA

(1) Δ | V_{OD} | and Δ | V_{OC} | are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.
(2) This device meets the ANSI Standard RS-485 VOD requirements above 0°C only.
(3) This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

5.5 Switching Characteristics - Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω C_L = 50 pF See Fig 3	8		31	ns
$t_{t(OD)}$	Differential output transition time			12		ns
$t_{sk(p)}$	Pulse skew (| $t_{d(ODH)}$ − $t_{d(ODL)}$|)				6	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω See Figure 4			65	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω See Figure 5			65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω See Figure 4			105	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω See Figure 5			105	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.5.1 Symbol Equivalents

Data Sheet Parameter	RS-485
V_O	V_{oa}, V_{ob}
| V_{OD1} |	V_O
| V_{OD2} |	V_t (R_L = 54 Ω)
| V_{OD3} |	V_t (test termination measurement 2)
Δ | V_{OD} |	| | V_t | − | V_t | |
V_{OC}	| V_{OS} |
Δ | V_{OC} |	| V_{OS} - V_{OS} |
I_{OS}	None
I_O	I_{ia}, I_{ib}

5.6 Electrical Characteristics - Reciever

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V	I_O = -0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V	I_O = 8 mA	-0.2(2)			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	(see Figure 4)			50		mV
V_{IK}	Enable-input clamp voltage	I_I = -18 mA				-1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV I_{OH} = -400 µA	See Fig 6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV I_{OL} = 8 mA	See Fig 6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = -7			-0.8	mA
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				-100	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				-100	µA
r_I	Input resistance			12			kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No Load	Receiver disabled and driver enabled			3.9	mA
			Receiver and driver disabled			0.25	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

5.7 Switching Characteristics - Reciever

over operating free-air temperature range (unless otherwise noted), C_L = 15 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level single-ended output	V_{ID} = -1.5 V to 1.5 V See Figure 7	11		37	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output		11		37	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)				10	ns
t_{PZH}	Output enable time to high level	See Figure 8			35	ns
t_{PZL}	Output enable time to low level				35	ns
t_{PHZ}	Output disable time from high level	See Figure 8			35	ns
t_{PLZ}	Output disable time from low level				35	ns

Parameter Measurement Information

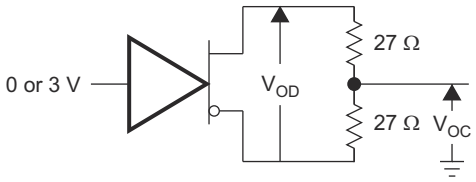


Figure 6-1. Driver V_{OD} and V_{OC}

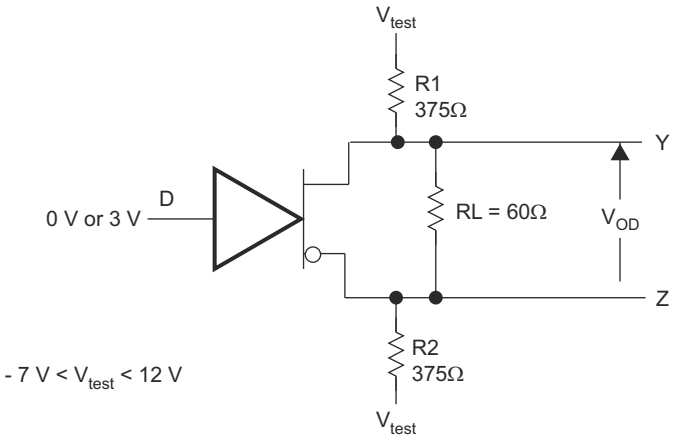
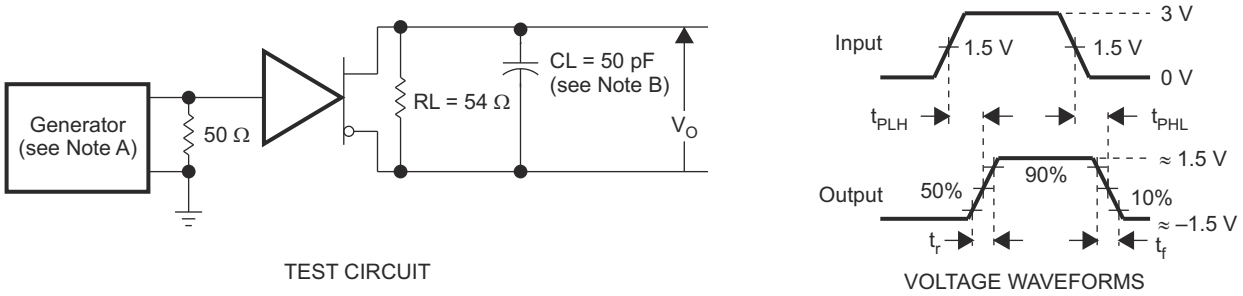


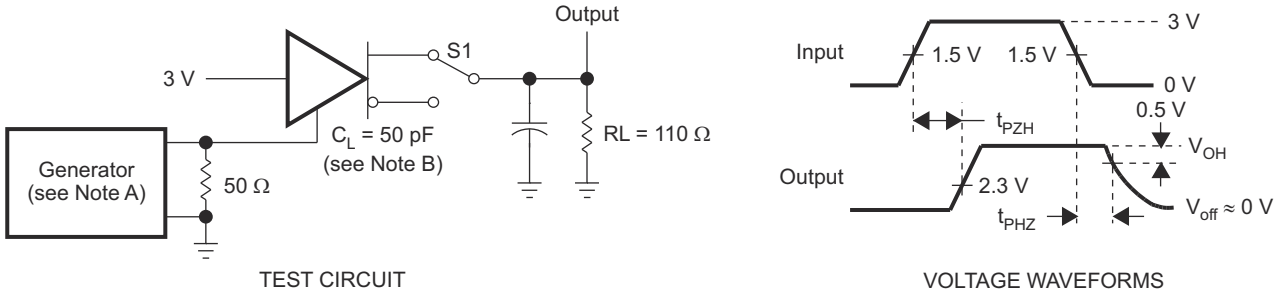
Figure 6-2. Driver V_{OD3}



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

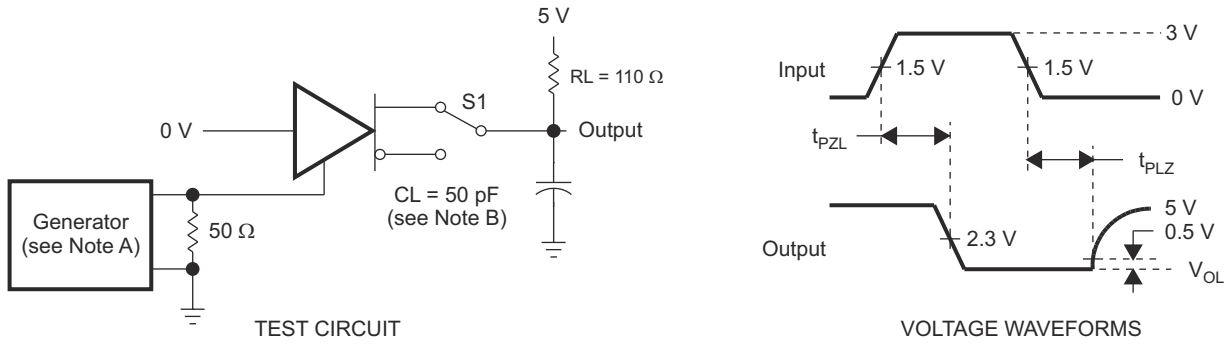
Figure 6-3. Driver Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-4. Driver Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-5. Driver Test Circuit and Voltage Waveforms

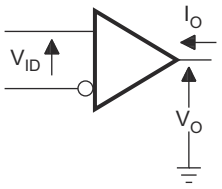
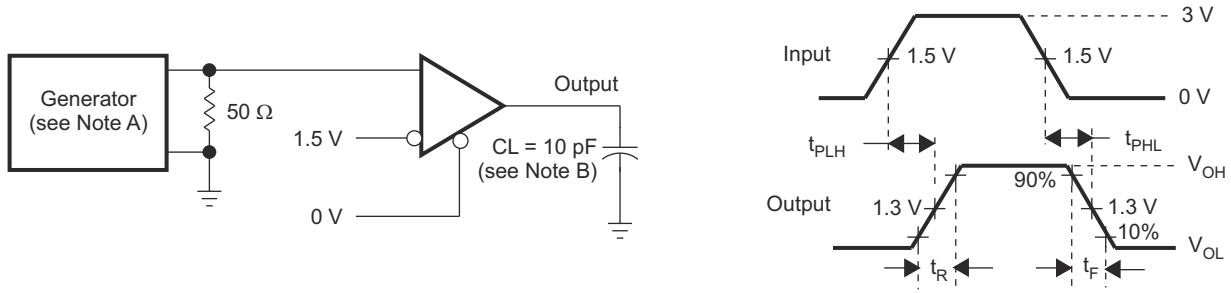


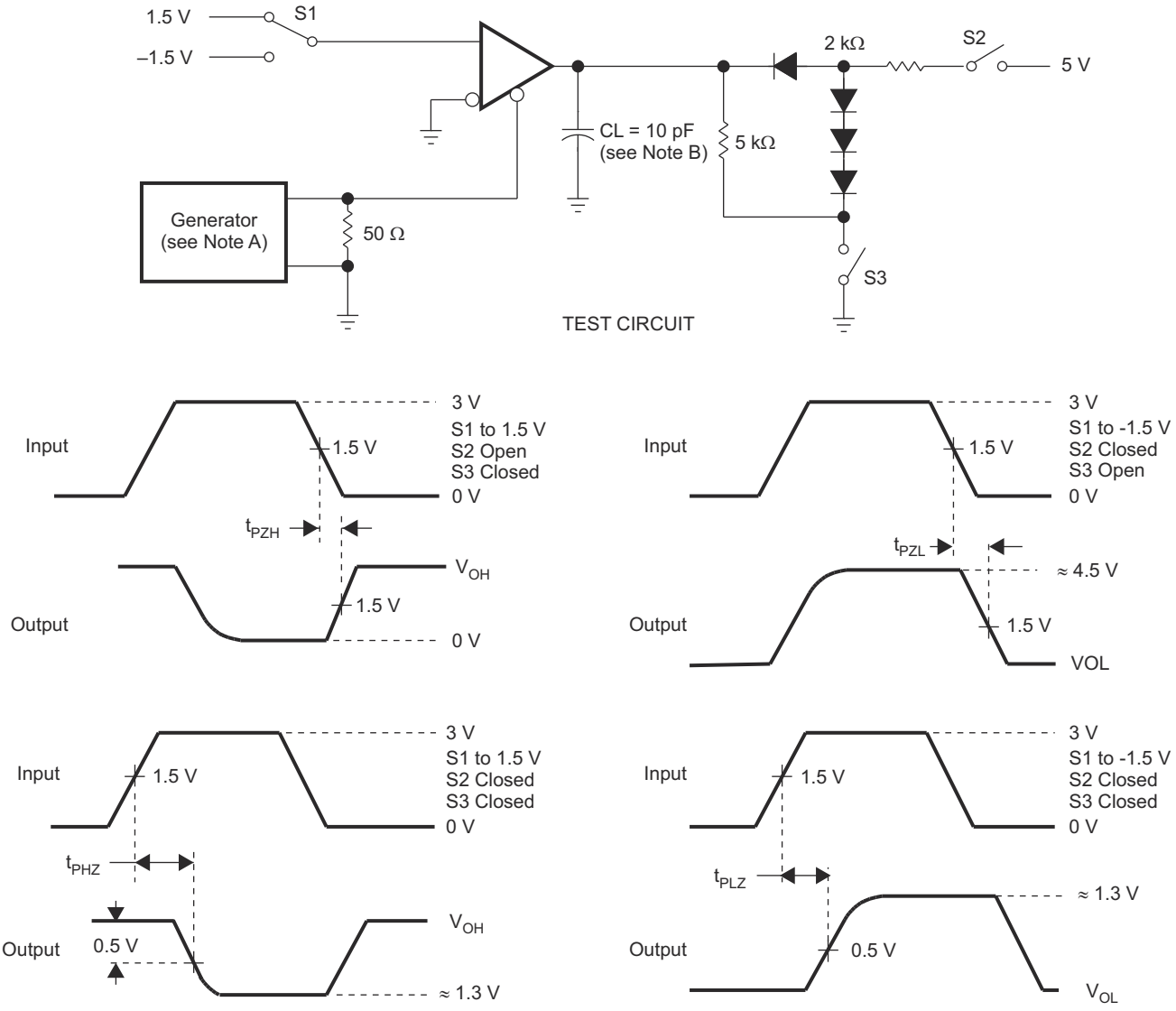
Figure 6-6. Receiver V_{OH} and V_{OL}



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-7. Receiver Test Circuit and Voltage Waveforms



VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-8. Receiver Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Device Functional Modes

Table 6-1. Function Table - Driver

Input(1)	Output	Outputs	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

Table 6-2. Function Table - Receiver

Differential Inputs	ENABLE	Output
A−B	$\overline{RE}$	R
VID ≥ 0.2 V	L	H
−0.2 V < VID < 0.2 V	L	?
VID ≤ − 0.2 V	L	L
X	H	Z
Open	L	H

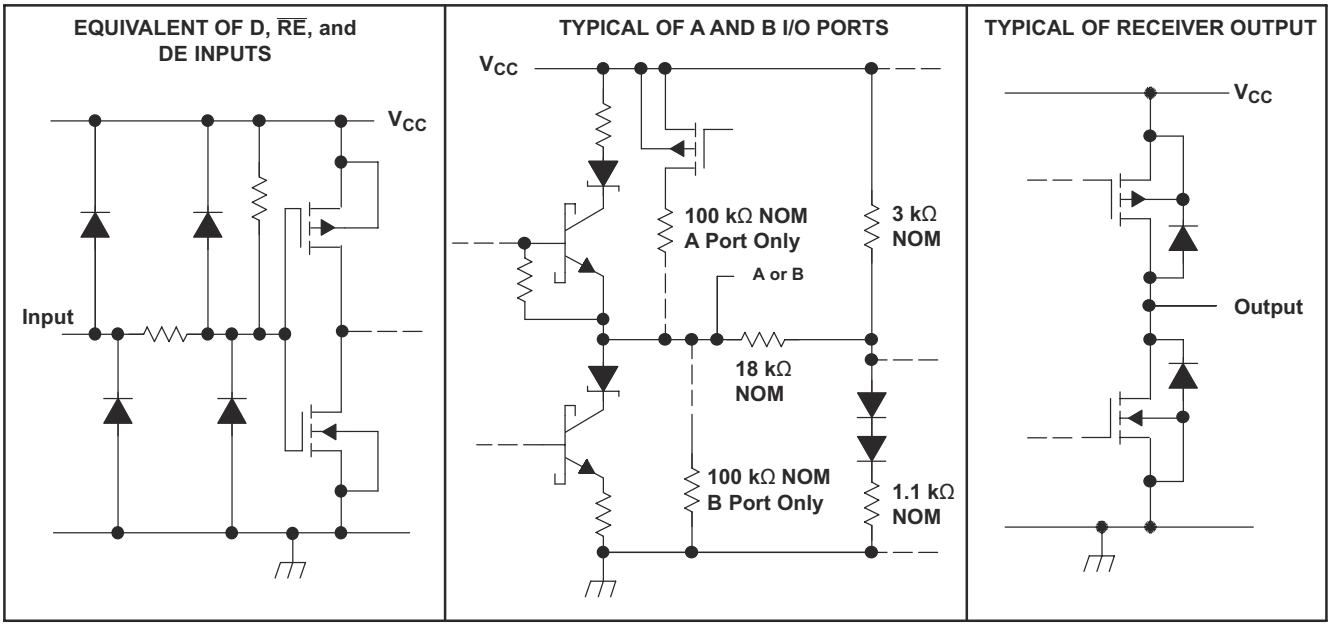


Figure 6-1. Schematics of Inputs and Outputs

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC176QDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J176Q1	Samples
SN65LBC176QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J176Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN65LBC176-Q1 :

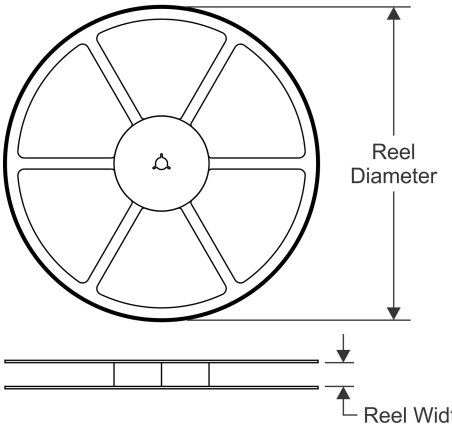
- Catalog: SN65LBC176

NOTE: Qualified Version Definitions:

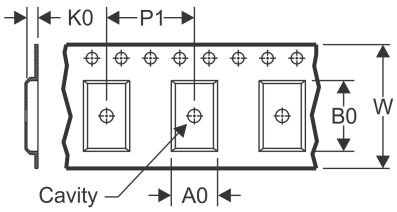
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

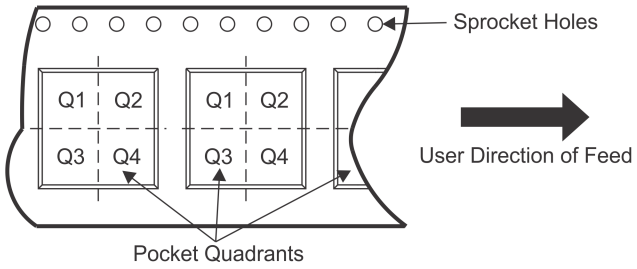


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

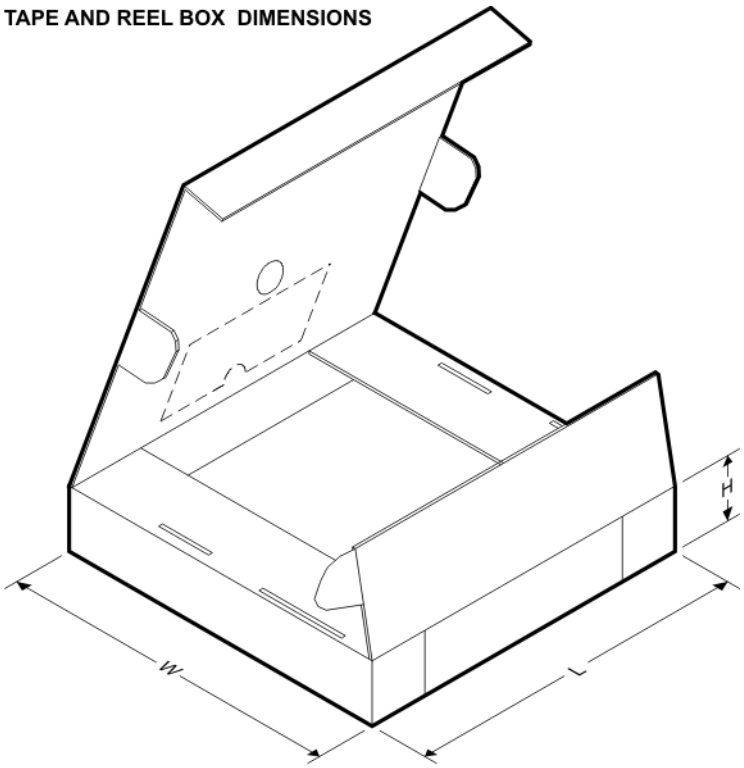
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

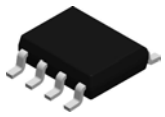
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176QDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176QDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0

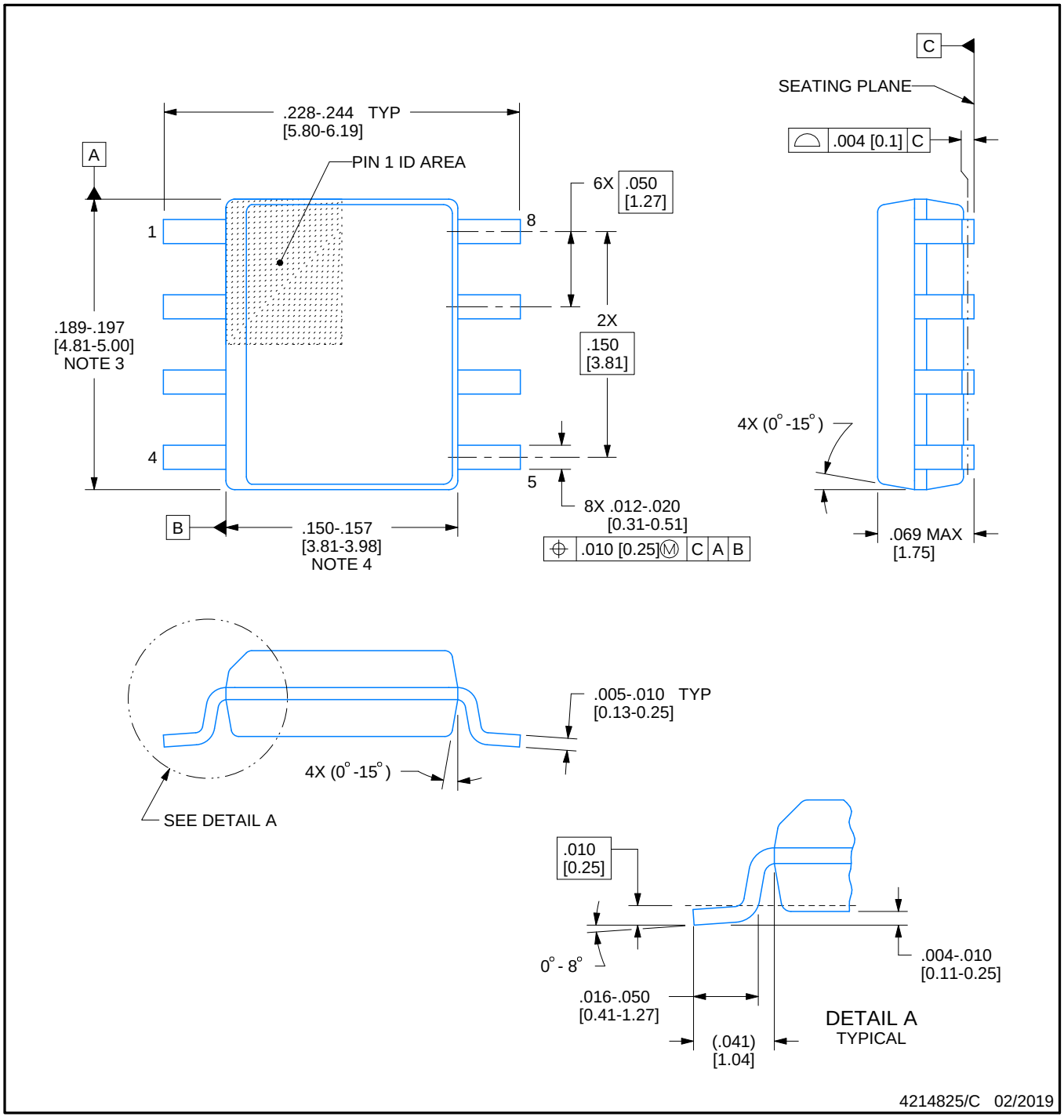


PACKAGE OUTLINE

D0008A

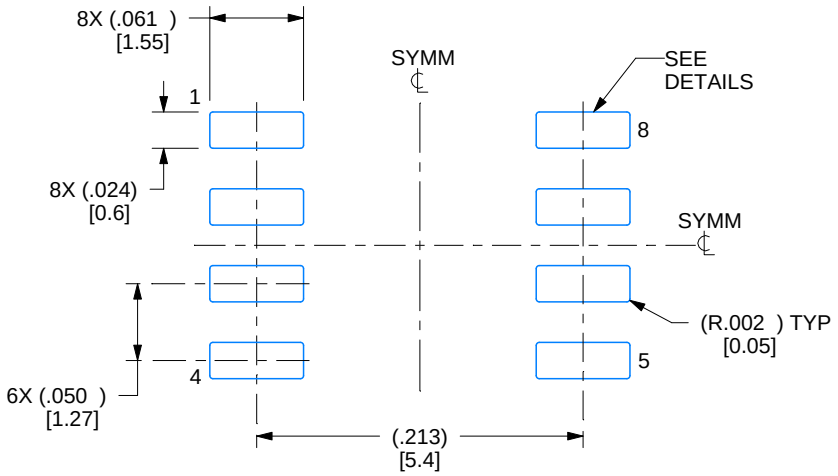
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

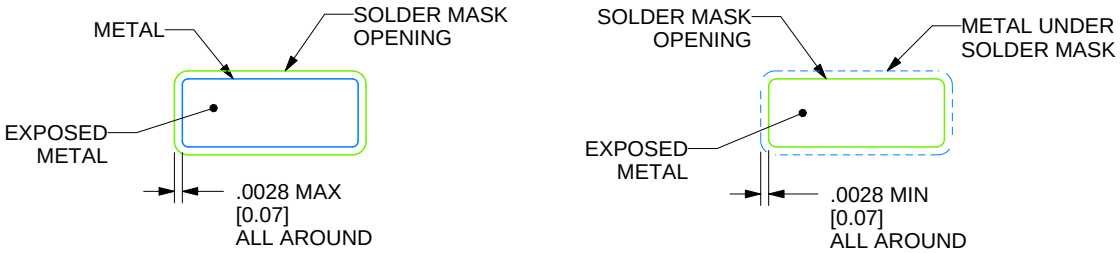


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

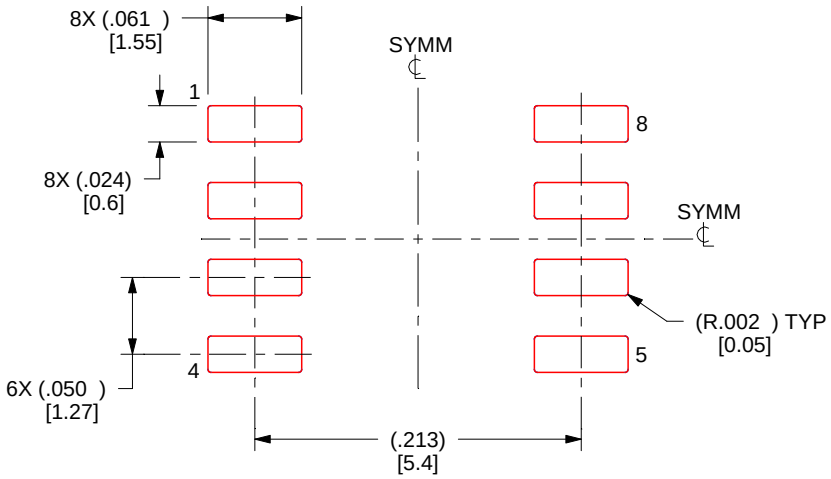
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265