Low Noise, Medium Current, High IP3

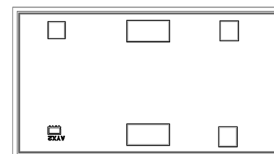
E-PHEMT Transistor Die

TAV2-501-D+

50Ω 0.4 to 3.9 GHz

The Big Deal

- Single Positive Supply Voltage
- Low Noise Figure, 0.6 dB at 0.9 GHz
- Gain, 15 dB at 2 GHz
- High Output IP3, 43 dBm at 2 GHz
- P1dB, 30.6 dBm at 0.9 GHz, 27.7 dBm at 2 GHz
- External biasing and matching required



Product Overview

Mini-Circuits' TAV2-501-D+ is a MMIC E-PHEMT* transistor die with an operating frequency range from 0.4 to 3.9 GHz. It has outstanding Noise Figure, particularly below 2.5 GHz, and when combining this noise figure with high IP3 performance in a single device it makes it an ideal amplifier for demanding cellular infrastructure.

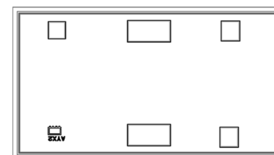
Key Features

Feature	Advantages
Wideband, 0.4 to 3.9 GHz	A single device covers many wireless communications bands including cellular, ISM, GSM, WCDMA, WiMax, WLAN, and more.
High IP3 vs. DC power consumption • +42.9 dBm at 0.9 GHz • +42.9 dBm at 2 GHz • +43.9 dBm at 3.9 GHz For additional data, see Tables 1-4 on Page 5	The TAV2-501-D+ matches industry leading IP3 performance relative to device size and power consumption. Enhanced linearity over a broad frequency range makes the device ideal for use in: • Driver amplifiers for complex waveform up converter paths • Drivers in linearized transmit systems
High P1dB • +30.6 dBm at 0.9 GHz • +27.7 dBm at 2 GHz • +30.0 dBm at 3.9 GHz For additional data, see Tables 1-4 on Page 5	Results in a very dynamic range preventing amplifier saturation under strong interfering signals.
Combines high gain (23.5 dB) with very low Noise Figure (0.6 dB)	The unique combination of high gain and low Noise Figure results in lower overall system noise.
Unpackaged Die	Enables the user to integrate the amplifier directly into hybrids

* Enhancement mode Pseudomorphic High Electron Mobility Transistor.

E-PHEMT Transistor Die TAV2-501-D+

Product Features
- Single Positive Supply Voltage
- Low Noise Figure, 0.6 dB at 0.9 GHz
- Gain, 15 dB at 2 GHz
- High Output IP3, 42.9 dBm at 2 GHz
- P1dB, 30.6 dBm at 0.9 GHz, 27.7 dBm at 2 GHz
- External biasing and matching required



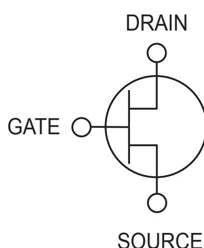
Typical Applications
- Cellular
- ISM
- GSM
- WCDMA
- WiMax
- WLAN

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Ordering Information: Refer to Last Page

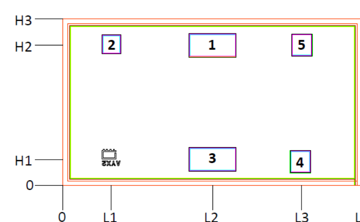
General Description
Mini-Circuits' TAV2-501-D+ is a MMIC E-PHEMT* transistor die with an operating frequency range from 0.4 to 3.9 GHz. It has outstanding Noise Figure, particularly below 2.5 GHz, and when combining this noise figure with high IP3 performance in a single device it makes it an ideal amplifier for demanding cellular infrastructure.

Simplified Schematic and Pad description



Pad#	Description
1 & 5	GATE used for RF-IN
2 & bottom of die	SOURCE Terminal, normally connected to ground
3 & 4	DRAIN used for RF-OUT

Bonding Pad Position



Dimensions in µm, Typical

L1	L2	L3	L4	H1	H2	H3
154	475	759	950	84	446	530

Thickness	Die size	Pad Size 1 & 3	Pad size 2	Pad Size 4 & 5
100	950 x 530	144 x 69	301 x 69	59 x 64

Electrical Specifications at T_{AMB}=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
		DC Specifications				
V_{TH}	Threshold Voltage	V_{DS}=4.5V, I_{DS}=28 mA		0.38		V
I_{DSS}	Saturated Drain Current	V_{DS}=4.5V, V_{GS}=0 V	—	0.5	—	µA
G_M	Transconductance	=4.5V, Gm =$\Delta I_{DS}/\Delta V_{GS}$, $\Delta V_{GS} = V_{GS1}-V_{GS2}$, $V_{GS1}=V_{GS\ typ}$-0.05 $V_{GS2}=V_{GS\ typ}$-0.05	—	2600	—	mS
I_{GSS}	Gate leakage Current	$V_{GD}=V_{GS}$=-6.7V	—	65		µA

RF & DC Specifications, Z0=50 Ohms					
Parameter	Condition (GHz)	V_{DS} = 4.5V, I_{DS} = 280mA			Units
		Min.	Typ.	Max.	
Gain	0.9		23.5[2,4]		dB
	2.0		15.1[3]		
P1dB	0.9		30.6[2,4]		dBm
	2.0		27.7[3]		
OIP3 Pout=0dBm/Tone	0.9		42.9[2,5]		dBm
	2.0		42.9[3]		
Noise Figure	0.9		0.6[1]		dB
	2.0		1.3[3]		
Power Added Efficiency	0.9		45[2,4]		dB
	2.0		45[3]		
I_{DS}	DC		280		mA
V_{GS}	DC	0.39	0.52	0.65	V

1. For measurements at 0.9 GHz, die is packaged in 2x2mm, 8-lead MCLP package and soldered on Mini-Circuits characterization board TB-TAV2-501+ with no optimization.
2. For measurements at 0.9 GHz, die is packaged in 2x2 mm, 8-lead MCLP package and soldered on Mini-Circuits characterization board TB-TAV2-501+ with load and source pull test (See Fig. 1).
3. For measurements at 2 GHz, die is packaged in 2x2 mm, 8-lead MCLP package and soldered on Mini-Circuits matching circuit test board TB-TAV2-501M+ (See Fig. 2).
4. Measurements at 0.9 GHz obtained for optimized P1dB. Die is packaged in 2x2mm, 8-lead MCLP package and soldered on Mini-Circuits characterization board TB-TAV2-501+.
5. Measurements at 0.9 GHz obtained for optimized IP3. Die is packaged in 2x2mm, 8-lead MCLP package and soldered on Mini-Circuits characterization board TB-TAV2-501+.

Absolute Maximum Ratings[1,2,3,6]

Symbol	Parameter	Max.	Units
V_{DS}[7]	Drain-Source Voltage	7	V
V_{GS}[7]	Gate-Source Voltage at V_{DS}=4.5V	-5 to +0.8	V
I_{DS}[7]	Drain Current at V_{DS}=4V	500	mA
I_{GS}	Gate Current	60	µA
P_{DISS}	Total Dissipated Power	2.4	mW
P_{IN}[8]	RF Input Power	28	dBm
T_{CH}	Channel Temperature	150	°C
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STD}	Storage Temperature	-65 to 150	°C
θjc	Thermal Resistance	23	°C/W

6. Operation of this device above any one of these parameters may cause permanent damage.
7. Assumes DC quiescent conditions.
8. I_{GS} is limited to 60µA during test.

Characterization Test Circuit

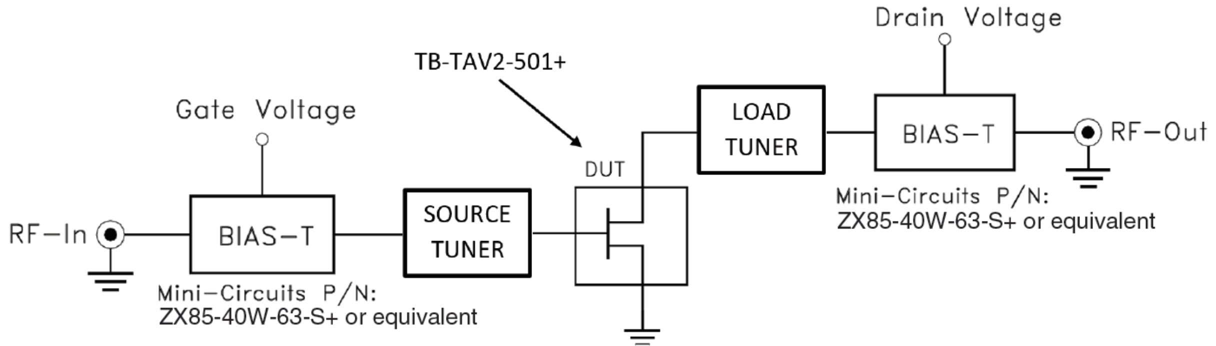
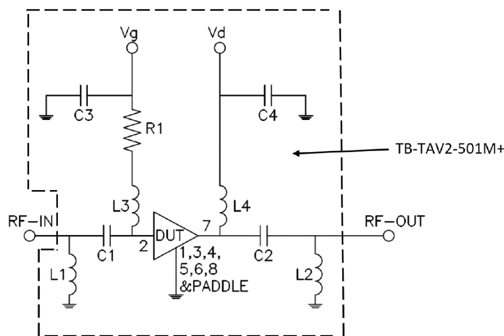


Fig 1. Block Diagram of Test Circuit used for characterization. (Die is packaged in 2x2 mm, 8-lead MCLP package and soldered on Mini-Circuits Test Board TB-TAV2-501+) Gain, Output power at 1dB compression (P1 dB) and output IP3 (OIP3) are measured using Keysight Network Analyzer N5424A PNAx and Maury automated tuner.

Conditions (Optimized IP3):
1. Drain voltage (with reference to source, VDS) = 4.5V as shown.
2. Gate Voltage (with reference to source, VGS) is set to obtain desired Drain-Source current (IDS) as shown in specification table or load and source pull tables.
3. Gain: Pin= -25dBm
4.Pin for IP3: -10 dBm at 0.9 GHz, -5 dBm at 2.0 GHz, -1 dBm at 2.4 GHz, 0 dBm at 3.9 GHz.

Conditions (Optimized P1dB):
1. Drain voltage (with reference to source, VDS) = 4.5V as shown.
2. Gate Voltage (with reference to source, VGS) is set to obtain desired Drain-Source current (IDS) as shown in specification table or load and source pull tables.
3. Gain: Pin= -25dBm
4. Pin for IP3: -10 dBm at 0.9 GHz, -5 dBm at 2.0 GHz and 2.4 GHz, -2 dBm at 3.9 GHz.

Recommended Application Circuit



VDS, V (nom)	4.5
IDS, mA (nom)	280
R1	15 Ω
C1	2.4 pF
C2	2.4 pF
C3	2.2 µF
C4	2.2 µF
L1	1.2 nH
L2	1.5 nH
L3	15 nH
L4	47 nH

Fig 2. Recommended Application Circuit used for characterization. (Die is packaged in 2x2 mm, 8-lead MCLP package and soldered on Mini-Circuits Matching Circuit Test Board TB-TAV2-501M+)

Table 1: Optimum OIP3 at 4.5 V, 280 mA

Freq (GHz)	OIP3 (dBm)	Gain (dB)	P1dB (dBm)	PAE (%)	Γ_{source}	Γ_{load}
0.9	45.11	19.98	29.85	49.66	0.694 ∠ - 114.29°	0.693 ∠ - 91.12°
2.0	46.32	14.22	28.68	48.82	0.842 ∠ 29.84°	0.715 ∠ 35.13°
2.4	44.64	11.23	27.44	42.12	0.724 ∠ 123.43°	0.638 ∠ 75.56°
3.9	43.89	11.00	27.83	42.76	0.884 ∠ - 108.07°	0.679 ∠ - 114.78°

Table 2: Optimum P1dB at 4.5 V, 280 mA

Freq (GHz)	OIP3 (dBm)	Gain (dB)	P1dB (dBm)	PAE (%)	Γ_{source}	Γ_{load}
0.9	40.18	22.77	30.03	52.30	0.658 ∠ - 87.51°	0.690 ∠ - 73.64°
2.0	41.52	17.02	30.23	56.73	0.743 ∠ 39.55°	0.715 ∠ 43.14°
2.4	41.11	15.10	30.52	53.56	0.742 ∠ 92.52°	0.720 ∠ 93.56°
3.9	39.53	11.72	29.95	46.67	0.759 ∠ - 95.66°	0.687 ∠ - 96.87°

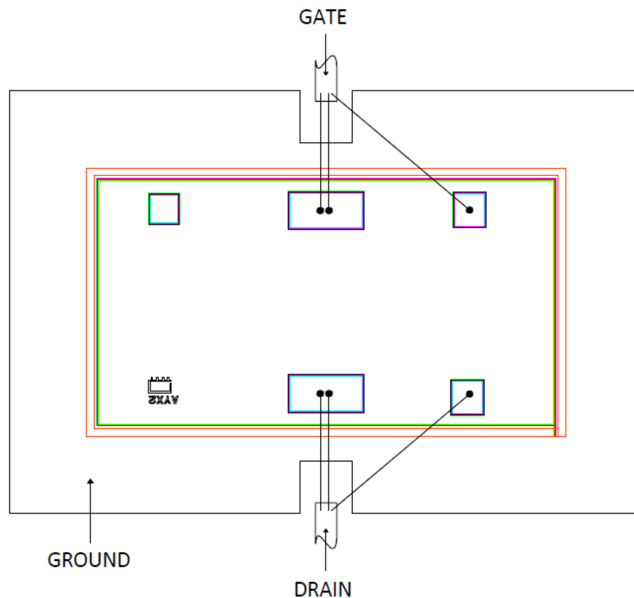
Table 3: Optimum OIP3 at 4.5 V, 400 mA

Freq (GHz)	OIP3 (dBm)	Gain (dB)	P1dB (dBm)	PAE (%)	Γ_{source}	Γ_{load}
0.9	47.67	16.84	29.54	50.28	0.645 ∠ - 138.14°	0.602 ∠ - 69.95°
2.0	45.77	15.97	29.23	50.14	0.649 ∠ 40.96°	0.613 ∠ 40.33°
2.4	48.05	13.40	29.66	48.74	0.803 ∠ 112.01°	0.619 ∠ 92.12°
3.9	46.32	11.40	29.57	46.28	0.884 ∠ - 108.07°	0.684 ∠ - 105.84°

Table 4: Optimum P1dB at 4.5 V, 400 mA

Freq (GHz)	OIP3 (dBm)	Gain (dB)	P1dB (dBm)	PAE (%)	Γ_{source}	Γ_{load}
0.9	42.99	23.04	30.01	45.83	0.658 ∠ -87.51°	0.785 ∠ - 87.47°
2.0	42.01	18.53	30.68	48.45	0.833 ∠ 43.23°	0.827 ∠ 42.17°
2.4	44.45	17.26	30.16	55.62	0.874 ∠ 94.67°	0.726 ∠ 86.88°
3.9	43.13	12.90	30.83	49.36	0.875 ∠ -101.14°	0.784 ∠ - 99.28°

Assembly Diagram



Assembly and Handling Procedure

1. Storage
   Dice should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC E-PHEMT transistor dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be opened in clean room conditions at an appropriately grounded anti-static worksta tion. Devices need careful handling using correctly designed collets, vacuum pickup tips or sharp antistatic tweezers to deter ESD damage to dice.
3. Die Attach
   The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are DieMat DM6030HK-PT/H579 or Ablestik 84-1LMISR4. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total die periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. It is recommended to use antistatic die pick up tools only.
4. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermosonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1 mil diameter. Bonds must be made from the bond pads on the die to the package or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

Additional Detailed Technical Information *additional information is available on our dash board.*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set
Case Style	Die
Die Ordering and packaging information	Quantity, Package — Model No. Small, Gel - Pak: 5,10,50,100 KGD* — TAV2-501-DG+ Medium†, Partial wafer: KGD*<2160 — TAV2-501-DP+ Large†, Full Wafer — TAV2-501-DF+ †*Available upon request contact sales representative* Refer to AN-60-067
Environmental Ratings	ENV80

*Known Good Dice ("KGD") means that the dice in question have been subjected to Mini-Circuits DC test performance criteria (VDS = 2V, ID = 214 mA) and measurement instructions and that the parametric data of such dice fall within a predefined range. While DC testing is not definitive, it does help to provide a higher degree of confidence that dice are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

ESD Rating**

Human Body Model (HBM): Class 1B (500V to <1000V) in accordance with ANSI/ESD STM 5.1 - 2001

** Tested in industry standard 2x2 mm, 8-Lead MCLP package.

Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

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